Design Procedure for High-Efficiency Linear Microwave Power Amplifiers

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Abstract—**An optimal design for a high-efficiency linear amplifier is achieved by a graphical technique, with the active device characterized by load impedance contours for constant power and constant intermodulation distortion (IMD). The use of this method is demonstrated by an example. Also described are the excellent results obtained in an amplifier operating over the frequency range from 3.7 to 4.2 GHz.**

I. Introduction

LINEAR OPERATION in amplifiers is achieved by reducing the RF input power to a level sufficiently low to avoid saturation of the active devices. When a high degree of linearity is required, this "back-off" mode of operation inevitably results in a low value of efficiency and output power. For any amplifier there is always a clear tradeoff between the degree of linearity and the value of efficiency, or output power, at a constant power supplied to the amplifier. Since linear amplifiers are used in satellite transponders which are critically limited in input power, it is important to be able to develop amplifiers that achieve the required linearity at high efficiency. For instance, the efficiency of the amplifier described in Section III is approximately twice that of a TWT operating at the same intermodulation distortion. GaAs FET's were used in this design because of their unsurpassed performance when used in circuits designed for low intermodulation distortion and high efficiency [1].

Although the design method described in Section II is applicable to any linear amplifier, the design of GaAs FET linear amplifiers offers a unique challenge because of the following: 1) the intermodulation distortion (IMD) depends critically on the circuit impedance; and 2) the slope of the IMD characteristics versus RF drive differs from the normal 3:1 slope, typical for predominant third order distortion, often reaching values close to 8:1 [1]–[3]. Therefore, FET amplifiers are often very sensitive to overdrive [1] and only an accurate and systematic characterization of the active device coupled to a precise design method allows achievement of optimum performance from the FET's.

Volterra series are a powerful tool for analyzing nonlinear circuits [4] and they have been applied for predicting IMD performance of FET amplifiers [5]. This method, though, requires intensive use of a computer and is practical only for small nonlinearities. Larger nonlinearities can be analyzed by modeling the active device by means of a nonlinear equivalent circuit [3], [6]. The circuit performance under different conditions can then be studied with the aid of computer programs capable of handling nonlinear circuit elements. However, the technique is often inconvenient because these computer programs are generally large and expensive to run. In addition, the modeling of FET's, particularly those in a package, is often difficult.

What is missing is a simple but accurate practical design method for low-IMD amplifiers, one which could directly use IMD data obtained experimentally from active devices. The method described in this paper fills this need. It is based on a graphical technique that allows the designer to identify the optimum circuit impedance for maximum power and efficiency at any predetermined value of IMD. A systematic characterization of the active devices is used here in the form of impedance contours for constant power and constant IMD.

II. Design Method

It is the objective of this design method to determine that unique set of operating parameters which result in the device delivering the maximum output power at predetermined values of carrier-to-intermodulation ratio (C/I) and frequency. Parameters that are considered most important are: load impedance, RF input power, and bias. The method described herein determines the optimum load impedance and RF input power while the bias is held constant. Bias optimization requires either repeating the procedure at different bias levels or an experimental adjustment of the bias, starting from the condition which provides the maximum saturated power.

A consequence of the uniqueness of the set of optimum operating parameters is that an increase of RF drive will result in a decrease of output power at a predetermined C/I ratio, a decrease that cannot be overcome by changing the load impedance. Thus no tradeoff can be made between gain and maximum power at a predetermined C/I ratio.

For clarity, the design procedure will be illustrated in a specific design. The method can be easily extended to other devices and different applications.

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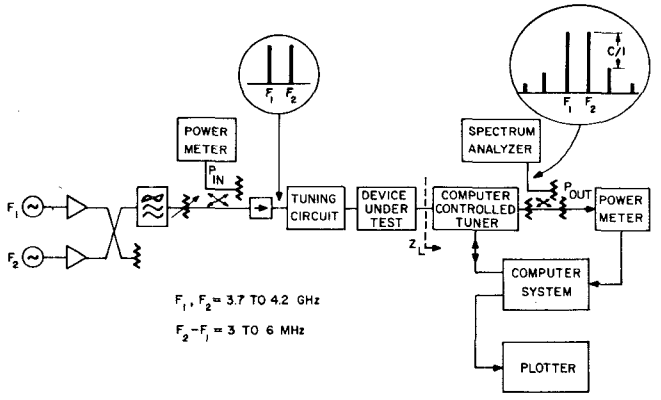

Fig. 1. Setup for measurement of constant power and IMD impedance contours.

A. Impedance Contours for Constant Output Power and IMD

For any active device such as, for instance, an FET or a bipolar transistor, there exists a critical value of load impedance which minimizes the device IMD. It has been shown that this load impedance differs from either the impedance for maximum saturated output power or the impedance for maximum gain [1], [7]. An active device characterization, particularly useful for the circuit design of the amplifier, is obtained here by plotting on a Smith chart impedance contours corresponding to constant output power and constant IMD. In our case these contours were measured with the aid of a computer-controlled tuner, similar to the one described in [8]. Fig. 1 is the block diagram of the measured setup. The signals from two generators are amplified by traveling wave tubes (TWT's), combined and fed to the input of the device under test through an input tuning circuit. The output of the device is connected to a load through the computer controlled tuner, constructed with a coaxial slotted line supporting small tuning elements on the center conductor. These elements, driven by stepping motors, can be positioned very accurately along the coaxial line. The load impedance Z_L, derived by the computer from the position of the elements, is then plotted on a Smith chart.

The intermodulation is measured by applying at the input of the device two equal-amplitude carriers separated by a few megahertz. The output signal contains the two amplified carriers plus unwanted intermodulation products. The harmonically related output signals are neglected here because, in most cases, they can easily be removed by filtering. A spectrum analyzer is used to measure the ratio C/I, in decibels, between the amplitude of the carriers and the highest intermodulation product. The total output power is read by the computer through a power meter.

Examples of the results from these experiments are shown in Figs. 2–4. The active device is a power FET, type MSC 88004 (Microwave Semiconductor Corporation), operated in class AB at a drain voltage of +8.0 V and a gate voltage of −1.66 V. Fig. 2 is the performance of the device tested with an input power of 16 mW at a frequency of 3.95 GHz. Each of the closed contours is the

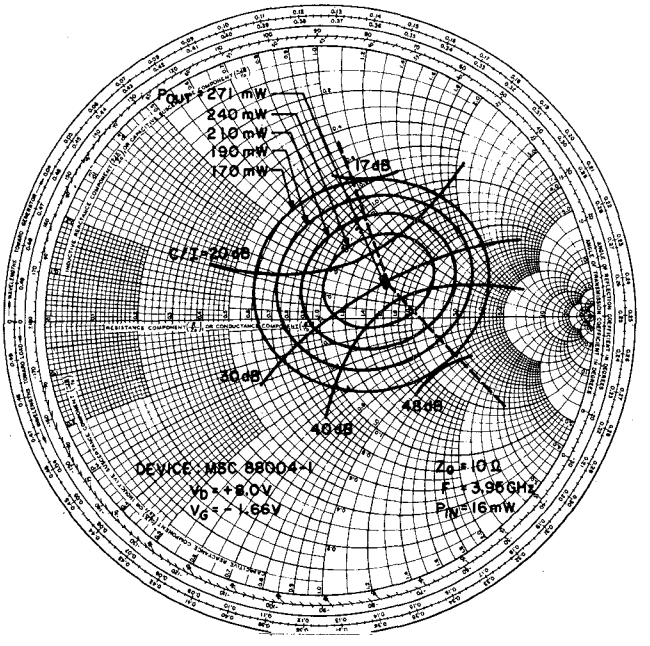

Fig. 2. IMD contours; $P_{in} = 16$ mW, $F = 3.95$ GHz.

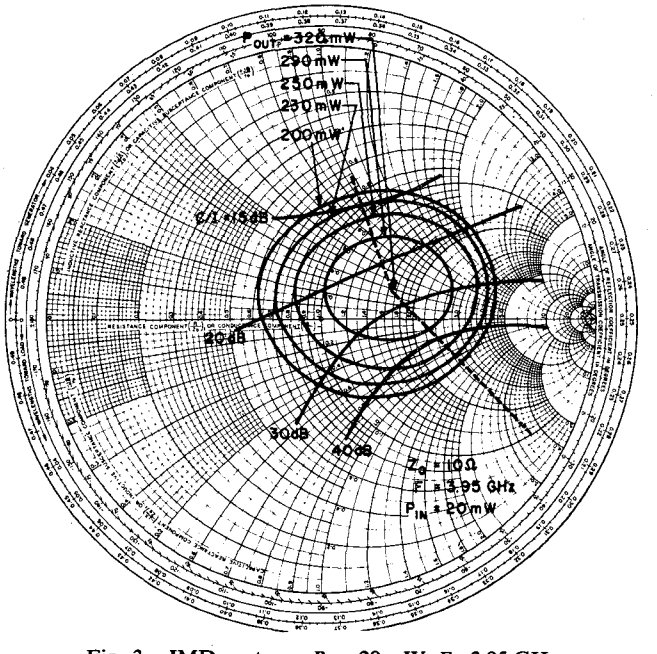

Fig. 3. IMD contours; $P_{in} = 20$ mW, $F = 3.95$ GHz.

locus of the drain-to-source load impedance Z_L, corresponding to a constant value of output power. The center of these contours, a contour itself degenerated into a single point, defines the load impedance which produces the maximum value of output power at a particular set of operating conditions, i.e., input power, frequency, and bias.

Each of the open contours is the locus of Z_L corresponding to a constant value of IMD, measured here by the carrier-to-intermodulation ratio C/I. These contours were obtained by measuring the C/I along the power contours and then by connecting points corresponding to equal values of C/I. This procedure requires a degree of

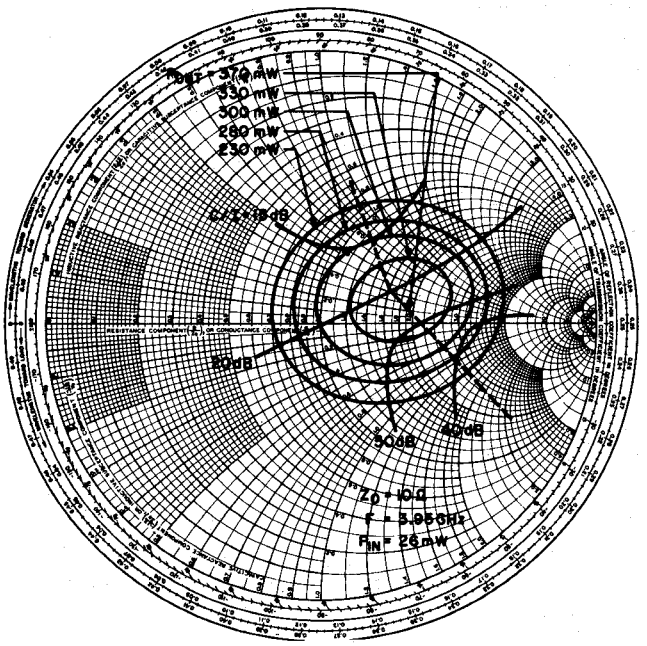

Fig. 4. IMD contours; $P_{in} = 26$ mW, $F = 3.95$ GHz.

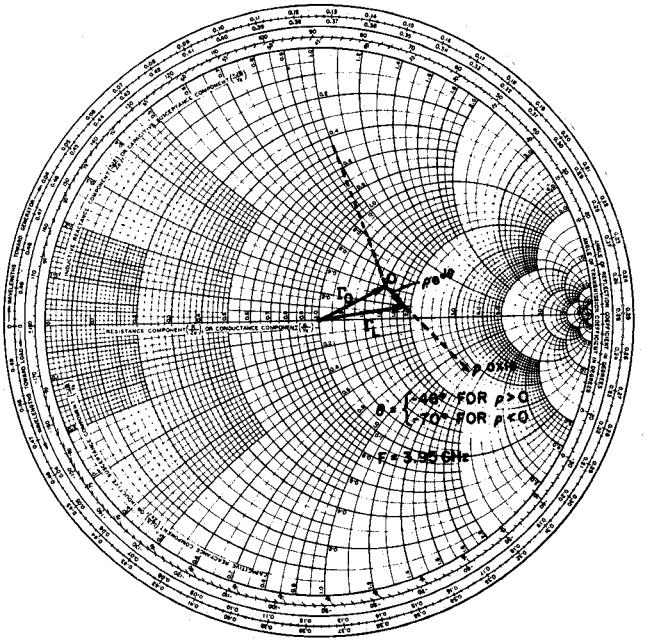

Fig. 5. Load impedance along optimum path.

manual intervention but, for ease of implementation, it was preferred to the automatic search of C/I contours. The values of load impedance required by this particular device are low and, in order to maintain good legibility on the Smith chart, the impedance plots of Figs. 2–4 were normalized to 10 Ω. Examples of power and IMD contours at increased RF input power levels are shown in Figs. 3 and 4.

It is clear from these measurements that intermodulation is critically dependent on the drain load impedance. For instance, a small change of this impedance, resulting in only a 0.3-dB variation of output power, can degrade the C/I ratio by as much as 10 dB. Thus, an accurate design method is needed, which defines the optimum load impedance for best IMD performance.

B. Optimum Load Impedance

One sees by inspection of Figs. 2–4 that along a line of constant intermodulation, the best load impedance corresponds to the point "closest" to the center of the power contours, since this load provides the maximum output power for a specified value of C/I. This condition is expressed more precisely by stating that the optimum load is defined by the tangent point between the C/I contour and the corresponding power contour. Notice that for a well-behaved device, only one power contour is tangent to one C/I contour; thus the tangent point is unique. The optimum path is now defined as the locus of the tangent points between the power and the C/I contours and being a gradient of both power and C/I contours, is that unique line perpendicular at any point to both contours. This common gradient line, approximated here for convenience by two straight lines, is shown in Figs. 2–4. Notice that, in general, the common gradient line or optimum path is a function of frequency. The reflection coefficient Γ_L of any point along this line can now be written as

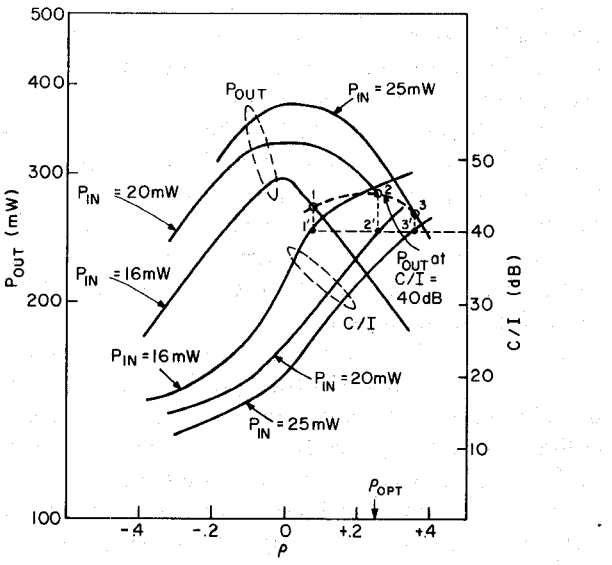

Fig. 6. Power and IMD versus load impedance.

$$\Gamma_L = \Gamma_0 + \rho^{j\theta}$$

where Γ_0 is the reflection coefficient of point 0, ρ is the distance of any point of the line from point 0, and θ is the angular position of the line. This is represented graphically in Fig. 5 for the center frequency. Note that the reflection coefficient of the load, represented by the complex number Γ_L, is now a function of a single independent real variable ρ.

The output power and the corresponding C/I ratio with the input power as a parameter can now be measured along the common gradient line and plotted as functions of ρ. These data, for the center frequency, are shown in Fig. 6. The curves in this figure are the vertical cross sections of the surfaces subtending the reflection coefficient plane (Smith chart) and describing output power

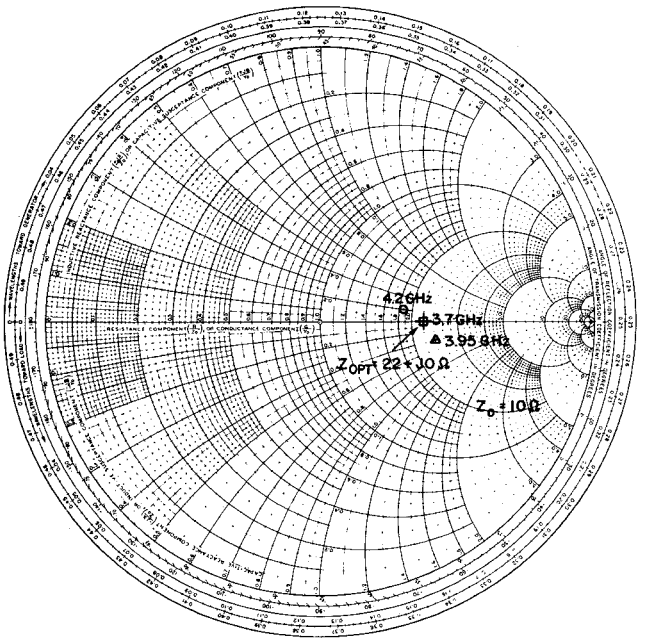

Fig. 7. Optimum load impedance versus frequency, MSC 88004.

and IMD as functions of load impendance and RF input power. The contours of Figs. 2–4, instead, are horizontal cross sections of the same surfaces.

The optimum load and input power are now determined as follows. A horizontal line at a specified value of C/I, 40 dB for instance, intercepts the C/I curves at the points 1′, 2′, and 3′. Vertical lines from each of these points to the P_{out} curves corresponding to the same P_{in} define points 1, 2, and 3. A curve can now be traced through these points which defines values of output power as a function of ρ at different levels of input power. The maximum of this curve defines ρ_{OPT} which in turn defines the optimum load impedance. At this point the set of optimum operating parameters—load impedance, RF input power, and bias—is uniquely defined.

The same design technique can easily be applied at different operating frequencies. As an example, the optimum impedance values obtained at 3.7 and 4.2 GHz are plotted in Fig. 7. It should also be noted that the design procedure described here is general and can be applied for any value of C/I.

III. FET Amplifier Performance

A. Amplifier Layout

The electrical schematic of the complete amplifier module is shown in Fig. 8. The RF signal, amplified by the driver stage, is split by the 3-dB coupler and feeds the inputs of the power amplifiers. The output powers from the two identical amplifiers are then recombined in the output coupler. The driver stage, designed for a C/I level (at nominal drive) of 55 dB, contributes 1.6 dB to the overall IMD. Thus the final amplifiers were designed for a C/I of 41.6 dB. The output circuits of these amplifiers were designed for an impedance of $22+j0$ ohms, approximately constant with frequency. The FET's were biased at approximately 1/2 of the saturation current.

The bias voltages are supplied to the devices through RF chokes having an inductance of approximately 20 nH. The RF signal at the "cold" side of the choke is bypassed by a low-loss 55-pF MOM (Metal–Oxide–Metal) capacitor [9]. Similar capacitors are also used as dc blocks along the RF circuits. High value electrolytic capacitors are connected in the bias circuit to bypass the modulation frequencies. Their connections to the bias circuit are kept to a minimum length in order to achieve a large modulation bandwidth [10].

Fig. 9 is a photograph of the amplifier with its cover removed. Each FET is fastened to the circuit tray by means of two screws. The *X*-shaped interdigitated quadrature couplers are connected at the input and output of the power stage. The bias RF chokes are connected to MOM capacitors soldered on the side wall of the circuit trays.

B. Measured Performance

The frequency response of the amplifier is shown in Fig. 10. Over the operating bandwidth the response is quite uniform: at 3 mW of input power, the gain is 22.5 ± 0.3 dB with an output power of 540 mW. The saturated output power, at 25 mW input, ranges from 1.5 to 1.8 W, and is also rather uniform over the operating bandwidth. Note that the same ratio exists between the 3-, 8.6-, and 25-mW input power levels; therefore, these results show clearly a saturation of the output power for input power levels above 8.6 mW.

The intermodulation performance was measured by applying two equal amplitude carriers 3 MHz apart at the input. The input and output power at 3.95 GHz, measured as the total power of the two carriers, and the power-added efficiency are plotted in Fig. 11 as functions of the C/I ratio. Over the range from 3.7 to 4.2 GHz, the output power at a C/I of 40 dB is remarkably constant, varying only from 510 to 520 mW. The corresponding power-added efficiency is 7.3 to 7.5 percent. Under these conditions the RF input power is 2.8 to 3.2 mW with an associated gain of 22.1 to 22.6 dB. An analysis of the output versus C/I curves shows that only for high values of C/I, greater than 40 dB for instance, is the slope of the C/I versus P_{out} curve 2:1. Thus, a change of output power by 1 dB results in a change of the C/I by 2 dB, which is expected from "linear amplifiers" when third order distortion is predominant. At lower values of C/I, however, the slope of the C/I curve changes drastically, reaching a typical value of 7.5:1. This is a direct consequence of operating the FET's in an area which is highly linear and yet near to saturation. Thus, even a relatively small overdrive can saturate the device and can greatly reduce the C/I ratio.

This amplifier operates in a class AB mode. Therefore, when a modulated RF signal is applied at the input, the currents in the bias circuits vary at the rate of the modulation frequency. It has been shown [10] that under these conditions the frequency limitation of the bias circuits

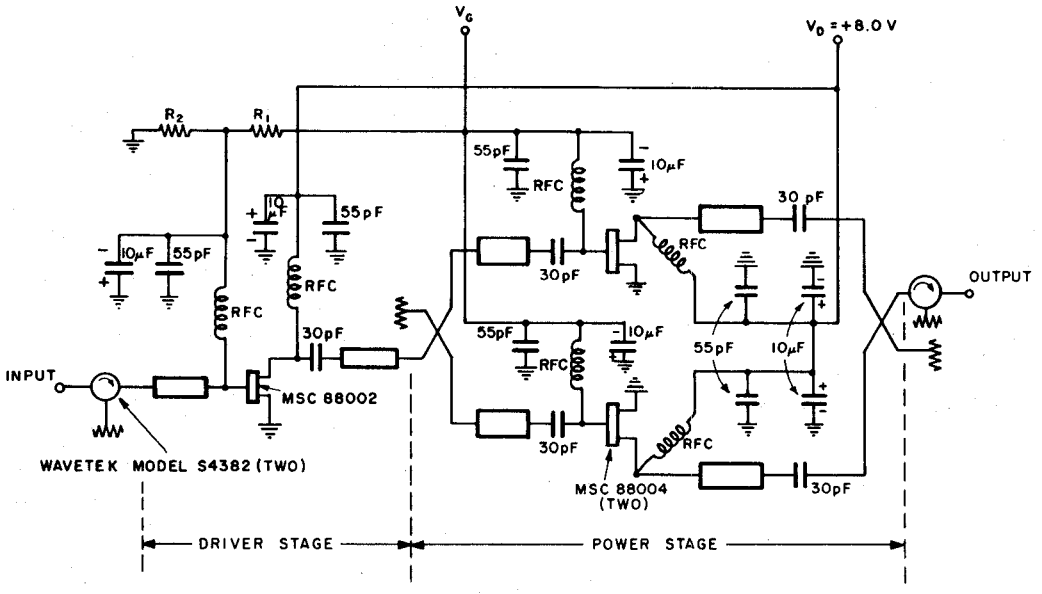

Fig. 8. Electrical schematic.

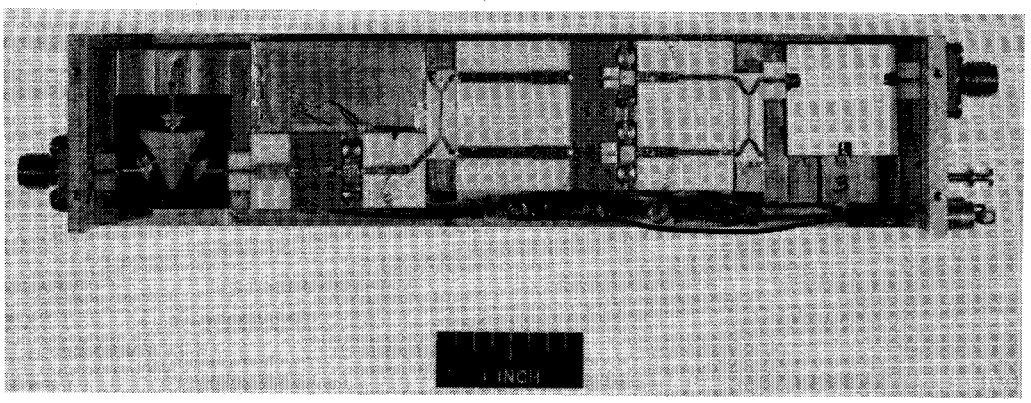

Fig. 9. Photograph of module.

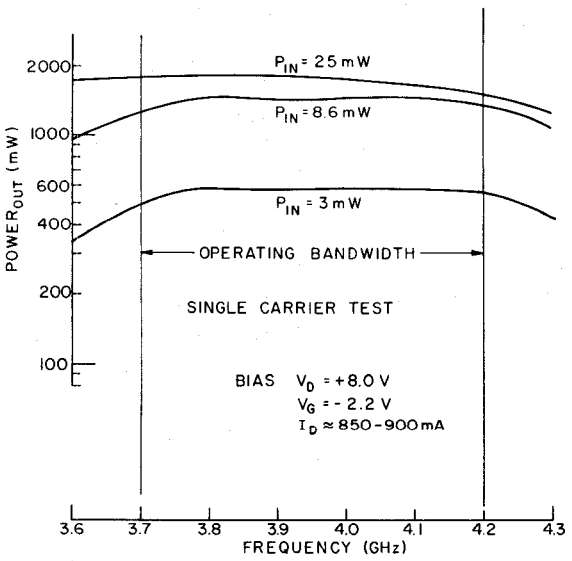

Fig. 10. Frequency response.

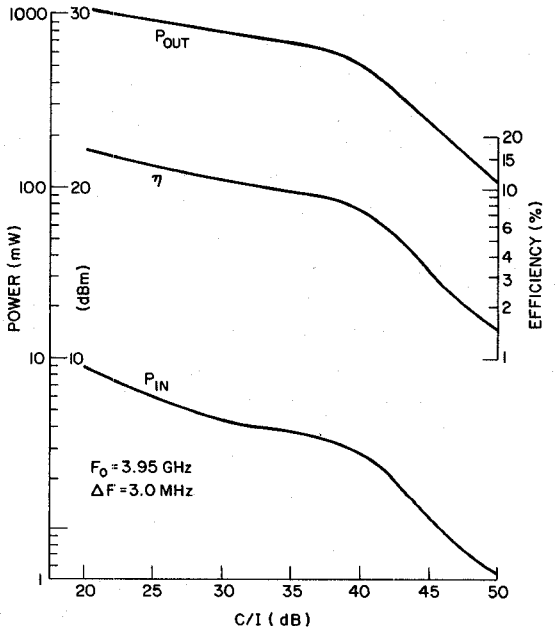

Fig. 11. IMD performance, 3.95 GHz.

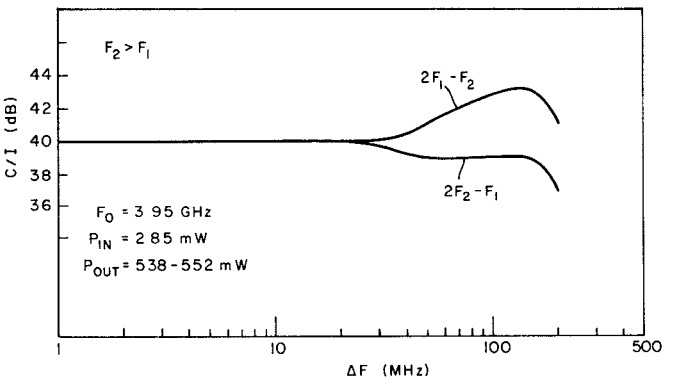

Fig. 12. IMD performance versus carrier separation.

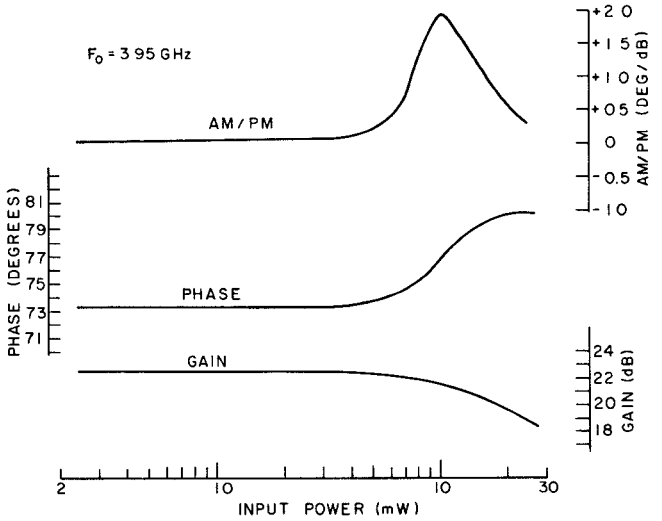

Fig. 13. Amplitude and phase characteristics at 3.95 GHz.

restricts the maximum modulation frequency and therefore also the maximum carrier separation in a two-carrier test. The measured intermodulation performance as a function of the carrier separation, ΔF, is shown in Fig. 12. The center frequency was kept at a constant value of 3.95 GHz. The levels of the two sidebands become unequal for a carrier separation of 25 MHz, which is consistent with the estimated cutoff frequency of the bias circuits. For carrier separations greater than 150 MHz, the average C/I ratio shows a marked tendency to decrease. Notice that at this point the sidebands fall at the edges of the operating bandwidth. Because of the high sensitivity of the intermodulation to the input drive (a 1-dB variation of the C/I can be caused by less than a 0.2-dB variation in input power), it is not clear whether the sideband unbalance is really caused by a limitation of the modulation bandwidth or, instead, is caused by an inevitable unbalance of the two input signals.

Amplitude and phase characteristics were also measured at different frequencies in the operating bandwidth. These single-carrier measurements were performed with the aid of a computer-controlled high-power network analyzer. The results at 3.95 GHz are plotted in Fig. 13 in the form of gain, phase and amplitude-modulation/phase-modulation (AM/PM) conversion as functions of the RF input power. When the input power is kept below 4 mW, the gain is almost constant and the AM distortion is small. Under these conditions, the phase is also almost constant, which results in low phase distortion (AM/PM $\simeq$0). When the RF drive is increased up to the point where the gain is compressed by approximately 1 dB, the phase reaches its highest sensitivity with input drive and the AM/PM conversion peaks reaching a value of 1.9°/dB. A further increment of the RF drive, which brings the amplifier further into saturation, results in a decrease of the AM/PM conversion because of decreased sensitivity of the amplifier to variations of the RF drive.

IV. Conclusions

A method for optimal design of linear power amplifiers was described, which allows the attainment of the highest output power and efficiency at specified values of intermodulation distortion. The first step in this method is the characterization of the active devices in terms of impedance contours for constant intermodulation and constant output power. The second step identifies the common gradient line between the power and the intermodulation contours. The third step is the plotting of the output power and the C/I as functions of the load impedance measured along the common gradient line. The fourth and last step is the plotting of the output power for a fixed value of intermodulation, which allows unique identification of the optimum load impendance. This systematic device characterization and design procedure is recommended when optimum intermodulation performance is of paramount importance. An optimal design is also relatively insensitive to variations of the active devices. For instance, the same circuit design used for different devices of the same type, resulted in IMD performances differing only 2 dB over the frequency range from 3.7 to 4.2 GHz.

The performance of the amplifier designed with this method was excellent: at a C/I of 40 dB the efficiency was 7.4–7.9 percent over the frequency range from 3.7 to 4.2 GHz with a gain of 22 dB and a power output of 500 mW. Even assuming the addition of a preamplifier to increase the overall gain to 60 dB, the efficiency at a C/I of 40 dB is approximately 1.8 times higher than that of a TWT amplifier operating at the same C/I ratio. Such a large saving in power consumption makes these highly-efficient linear FET amplifiers particularly useful for service in satellite transponders.

Acknowledgment

The author wishes to thank Dr. H. Huang for supplying the FET's used for the initial experiments on device characterization. Sincere appreciation also goes to Dr. V. Riginos of Comsat Laboratories and Dr. E. F. Belohoubek for the many stimulating discussions. The assembly of the amplifier was skillfully carried out by J. E. Brown and E. Mykietyn.

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Error Considerations in the Design of Microwave Transistor Amplifiers

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***Abstract*—In the design of microwave transistor amplifiers it is frequently of value to consider an idealization where the actual device is replaced by one with the reverse transfer parameter S_{12} set to zero, while other S-parameters remain unchanged. In this communication bounds are derived on errors which may result from use of such an idealization.**

I. Introduction

MANY DESIGN procedures for bipolar and field-effect microwave transistor amplifiers rely on the assumption that the reverse transfer parameter S_{12} may be set to zero while the remaining S-parameters are unchanged, e.g., [1], [2]. In this paper bounds are derived for the error which may be introduced as a result of this idealization. Conditions for the case of "zero error" between the gains from the "ideal" and "true" devices are also derived. Results are presented using S-parameter data for some representative microwave transistors, and amongst these examples the case of a potentially unstable device is included.

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II. Gain Relations

A. Gain Equalization

For the case of the amplifier layout of Fig. 1 the transducer power gain is [3]

$$G_T = \frac{|S_{21}|^2(1-|S_L|^2)(1-|S_g|^2)}{|1-S_gS_{11}-S_LS_{22}+S_LS_g\triangle|^2}, \qquad \triangle = S_{11}S_{22}-S_{12}S_{21} \tag{1}$$

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